1, which comprises:

a main memory as said memory means for storing coded image data for one video segment;

said decoding means for variable-length decoding said coded image data outputted from said main memory;

said block storing means, provided between said main memory and said decoding means so as to be capable of storing code strings for one block, for storing code strings for concatenated two blocks; and

depacking means, including said block storing means, for suitably combining required portions of sequentially supplied code strings to complete code strings for one block when code strings supplied from said main memory are not code strings for one block,

wherein said decoding means comprises:

a variable-length code table for storing a variable-length code for decoding said code strings for one block outputted from said block storing means; and

a barrel shifter for bit-shifting data for one block, which are outputted from said block storing means and which have been a lump of coded data before being depacking, on the basis of a code length, which is returned from said variable-length code table, and on the basis of bit information from a code address storing circuit, to supply the bit-shifted data to said variable-length code table.

5. A coded image data decoding system as set forth in claim 4, wherein said depacking means comprises:

said block storing means, provided between said depacking means and said decoding means, for storing said code strings for concatenated two blocks; and

code string concatenating means for suitably combining required portions of sequentially supplied code strings to concatenate code strings for one block when code strings supplied from said memory means are not code strings for one block, said code string concatenating means comprising a central processing unit.

6. A coded data decoding system as set forth in claim 4, wherein said decoding means further comprises:

a flag memory for storing, every area, a flag indicative of the fact that decoding of an area is completed at an EOB; and

a code address storing circuit for storing what number of bit of what number of byte the decoding of codes in an area ends.

7. A coded image data decoding system as set forth in claim 1, which comprises:

a main memory for storing coded image data for one video segment;

decoding means for decoding said coded image data supplied from said main memory;

depacking means comprising a register for reading coded image data for one block out of said main memory, and a CPU for controlling a depacking process so as to concatenate data for one block, which are read out of said main memory, to data for one block, which have been a lump of coded data before depacking said data for one block read by said register; and

a data bus for mediating the transmission of coded data between said main memory and said register,

wherein said decoding circuit comprises:

a variable-length code table for storing a variable-length code for decoding said code strings for one block outputted from said register; and

a barrel shifter for bit-shifting data strings for one block, which are outputted from said register and which are a lump of code strings before being depacking, on the basis of a code length, which is returned from said variable-length code table, and on the basis of bit information from a code address storing circuit, to supply the bit-shifted data to said variable-length code table.

8. A coded data decoding system as set forth in claim 7,

wherein said decoding means further comprises:

a flag memory for storing, every area, a flag indicative of the fact that decoding of an area is completed at an EOB; and

a code address storing circuit for storing what number of bit of what number of byte the decoding of codes in an area ends.

9. A coded image data decoding system as set forth in claim 1, which comprises:

a main memory for storing coded image data for one video segment;

decoding means for decoding said coded image data supplied from said main memory;

depacking means comprising a register for reading coded image data for one block out of said main memory, a code string concatenating circuit having two inputs and including the function of bit-shifting and concatenating the output contents of said register and the contents, which are inputted from said memory, to rewrite the results in said register and the function of being capable of changing the sequence of concatenation on the basis of the fact that the end conditions for a supplied block relate to first or second pattern, and a CPU for controlling a depacking process so that said register reads data for one block out of said main memory and said code string concatenating circuit concatenates the read data to data for one block; and

a data bus for mediating the transmission of coded data between said main memory and said depacking means,

wherein said decoding circuit comprises:

a variable-length code table for storing a variable-length code for decoding said code strings for one block outputted from said register; and

a barrel shifter for bit-shifting data strings for one block, which are outputted from said register and which are a lump of code strings before being depacking, on the basis of a code length, which is returned from said variable-length

code table, and on the basis of bit information from a code address storing circuit, to supply the bit-shifted data to said variable-length code table.

10. A coded data decoding system as set forth in claim 9, wherein said decoding means further comprises:

a flag memory for storing, every area, a flag indicative of the fact that decoding of an area is completed at an EOB; and

a code address storing circuit for storing what number of bit of what number of byte the decoding of codes in an area ends.

11. A coded image data decoding system as set forth in claim 1, wherein said block storing means comprises a buffer register capable of storing code data of 112 bits, and the frequency of accesses to said memory means is low.

12. A coded image data decoding system as set forth in claim 11, wherein the access of said 112-bit buffer register to a main memory serving as said memory means is only to read code data of 112 bits once to supply data of 16 bits.

13. A coded image data decoding method comprising the steps of:

storing code strings for at least one video segment in image data packed by an image compressing/decompressing format wherein the sum of the length of components other than variable-length code components in one block and the length of an end code is not shorter than a bit length obtained by subtracting 1 bit from the number of bits of the maximum length of variable-length code words;

fetching said code strings for at least one block at a time;

determining whether the fetched code strings for one block are arranged as a lump of block before depacking;

decoding the code strings for the block when the

determined block is the lump of block before depacking;

sequentially taking said code strings in blocks for the one video segment to concatenate code strings for the lump of block before depacking when the fetched code strings for one block are not arranged as the lump of block before depacking; and

decoding the concatenated code strings for one block.

14. A coded image data decoding method as set forth in claim 13, wherein said step of concatenating code strings inputs code strings so as to be capable of inputting two blocks, and decodes image data for additional one block to sequentially concatenate the code strings while storing image data for one block.

15. A coded image data decoding method as set forth in claim 13, wherein the contents of a block, in which a block end code indicative of the end of the block has not been detected, are temporarily rewritten in a memory.

16. A coded image data decoding method as set forth in claim 13, wherein said code strings for one video segment are read by a main memory to be processed, and said code strings for one block are processed by a 112-bit buffer register, the frequency of accesses between the main memory and the buffer register being low.

17. A coded image data decoding program comprising:

a procedure for storing code strings for at least one video segment in image data packed by an image compressing/decompressing format wherein the sum of the length of components other than variable-length code components in one block and the length of an end code is not shorter than a bit length obtained by subtracting 1 bit from the number of bits of the maximum length of variable-length code words;

a procedure for fetching said code strings for at least

one block at a time;

a procedure for determining whether the fetched code strings for one block are arranged as a lump of block before depacking;

a procedure for decoding the code strings for the block when the determined block is the lump of block before depacking;

a procedure for sequentially taking the code strings in blocks for the one video segment to concatenate the code strings for the lump of block before depacking when the fetched code strings for one block are not arranged as the lump of block before depacking; and

a procedure for decoding the concatenated code strings for one block.

18. A coded image data decoding program as set forth in claim 17, wherein said procedure for concatenating code strings inputs code strings so as to be capable of inputting two blocks, and decodes image data for additional one block to sequentially concatenate the code strings while storing image data for one block.

19. A coded image data decoding program as set forth in claim 17, wherein the contents of a block, in which a block end code indicative of the end of the block has not been detected, are temporarily rewritten in a memory.

20. A coded image data decoding program as set forth in claim 19, wherein said code strings for one video segment are read by a main memory to be processed, and said code strings for one block are processed by a 112-bit buffer register, the frequency of accesses between the main memory and the buffer register being low.